TRISTAN SDD

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CONTENT

- Silicon Drift Detector
- SDD for TRISTAN
- wafer level test
- integrated FET
- alternative readout
- next production
**Silicon Drift Detector (SDD)**

- **principle**
  - signal charge collection on small readout node by internal static electric field
  - X-ray spectroscopy → electron spectroscopy

- **large area**
  - 5 mm² ... 1 cm² (... wafer scale)
  - monolithic multi-channel option

- **small capacitance**
  - low noise, resolution close to Fano limit
  - high count rates

- **fully depleted and sensitive**
  - efficiency @ high energies (~ 10 keV)

- **backside illuminated, thin entrance window**
  - efficiency @ low energies (~ 100 eV)
  - peak/background ratio

- **integration of 1st amplifying FET**
  - further capacitance reduction
  - robust w.r.t. pickup & microphony
SDD FOR TRISTAN

- multichannel SDD
  - format: 166 (~ 14 x 12) cells
  - hexagonal cells
    - cell size: Ø ≈ 3 mm
    - cell area: A ≈ 7 mm²
  - bond pads placed at two chip edges

- small prototype formats
  - 47 (~ 8 x 6) cells
  - 12 (2 x 6) cells
  - 7 cells
  - single cells

- production volume
  - 6 wafers
  - + 2 wafers (alternative entrance window, stopped)
SDD FOR TRISTAN

- new layout feature
  - "standard" SDD
  - narrow FET
  - TRISTAN SDD

Dimensions are NOT in correct scale

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<td>Σ</td>
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Capacitance [pF] simulation/calculation/estimation
**Wafer Level Test**

- semi-automatic probe station with stepping function & flying probes

- devices
  - all wafers  - 4 x 166 cells
  - 2 wafers  - 4 x 47 cells  - 3 x 12 cells  - 4 x 7 cells

- test routine
  - ringX vs. ring1  2x (hemisphere)  integrated voltage divider
  - inner guard ring vs. drain  2x (hemisphere)  diode stability, shorts
  - reset diode vs. drain  14x (reset group)  diode stability, shorts
  - feedback cap vs. drain  166x (cell)  insulator integrity, shorts
  - source vs. drain  166x (cell)  transistor characteristics Id(Vds), contacts, shorts
  - source vs. bulk  166x (cell)  transistor characteristics Id(Vgs), contacts, shorts
  - back contact vs. bulk  1x (global)  diode stability, leakage current, depletion voltage
**Wafer Level Test**

- **entrance window diodes**
  - leakage current level of all formats scaled to 1 cm²
    - 20 ... 70 pA/cm²
    - depending on format
    - edge effect
  - high current @ low voltage
    - guard ring not functional
  - high current @ high voltage
    - ~ full depletion
    - interface current of opposite wafer surface
    - two material groups
      - w01, 02, 03
        \[ V_{\text{dep}} \approx 85 \ldots 100 \, \text{V} \]
      - w06, 07, 08
        \[ V_{\text{dep}} \approx 100 \ldots 110 \, \text{V} \]
**Wafer Level Test**

- **Integrated Transistor**
  - Wafer maps of transistor current
    - $I_s [\mu A] @ Vgs = 0 \text{ V}$

- **Strip Pattern**
  - Probably caused by implanter
  - Work-around by quad-mode
**Wafer Level Test**

- **summary**
  - all large format devices measured completely
    - 22 of 24 devices are defect-free
    - 2 defect hemispheres (inner guard ring diode)
  - small format devices
    - all devices of 2 wafers (8 x 007, 6 x 012, 8 x 047)
    - 22 of 22 devices are defect-free
**INTEGRATED FET**

- samples of all wafers, comparison with previous
  - saturation current
    \[ I_{DSS} = 323 \, \mu A \pm 20 \, \mu A \quad I_{DSS} = 358 \, \mu A \]
  - pinch-off voltage
    \[ V_{po} = -2.15 \, V \pm 0.05 \, V \quad V_{po} = -2.1 \, V \]
  - transconductance
    \[ g_m = \frac{\partial I_D}{\partial V_{GS}} \, (\text{at} \, I_D = 100 \, \mu A) \]
    \[ g_m = 157 \frac{\mu A}{V} \pm 8 \frac{\mu A}{V} \quad g_m = 174 \frac{\mu A}{V} \]
  - ac drain resistance
    \[ r_D = \frac{\partial V_{DS}}{\partial I_D} \, (\text{at} \, V_{DS} = 5 \, V) \]
    \[ r_D = 72 \, k\Omega \pm 6 \, k\Omega \quad r_D = 70 \, k\Omega \]
    \[ g_D = \frac{1}{r_D} \]
    \[ g_D = 13.8 \frac{\mu A}{V} \pm 1 \frac{\mu A}{V} \quad g_D = 14.3 \frac{\mu A}{V} \]
INTEGRATED FET

- SIMS measurement of channel implantations
  - comparison w.r.t. old production
ALTERNATIVE READOUT

- use of existing components (SDD 100 mm²)
  - module → Peltier cooled
    → SDD ceramic
  - SDD box → liquid cooling loop
    → low quality vacuum
    → foil window, $^{55}$Fe source
  - circuit → compact filter/amplifier board
    → source follower
    → commercial 2nd stage amplifier (AmpTek A250)
    → Gaussian filter
  - setup → chiller
    → individual power supplies
**ALTERNATIVE READOUT**

- **SDD readout**
  - most reduced & simplest circuit
    - source follower
    - discrete components
    - commercial preamp (AmpTek A250)
    - analog Gaussian filter
    - no pulsed reset, continuous gate discharge
    - no use of feedback cap

- **status**
  - module mounted
  - reanimation of setup next week
Next TRISTAN Production

- 2nd production required
  - number of devices
  - ? layout modifications?
- last launch window: beginning of 2021
- triggered by HLL move to new lab building
  - scheduled date: 1st half of 2022
  - delay conceivable, but not confirmed